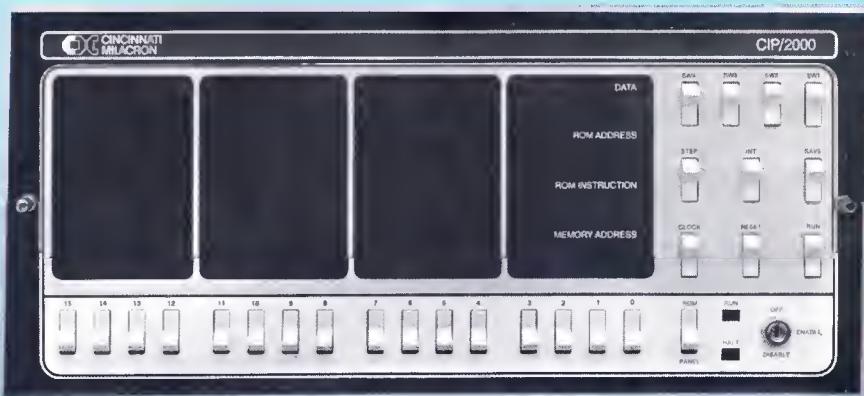


2100 HAS 50% OF ROM,  
22a SUPPOSED OF 2100  
S. KIM 11/18/71  
11/18/71

NOV 18 1971

2200 IS 80% OVER 2100

**CIP/2100**  
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## CIP/2100 MINICOMPUTER . . .

reliable, rugged, flexible, easy to use, economical.

Not just words to catch your eye, but the reasons why the CIP/2100 is the best general-purpose mini-computer for you.

The CIP/2100 was designed with the OEM user in mind. That's why the hardware is rugged and reliable, and the programming so flexible. "Easy to use" comes naturally with well-designed software, complete documentation, a people-oriented front panel, and for good measure, training courses in programming and maintenance. As for economical, a CIP/2100 is surprisingly low cost and a liberal OEM discount is available.

Good service isn't just a word either. Whether it's help with programming problems or on-time delivery you want or prompt field service, we've got the people and the skills to meet your needs.

## FEATURES

- Full memory cycle speed of 1.1 microseconds
- Hardware multiply and divide
- Expandable priority interrupt system
- 89 standard instructions
- I/O — serial, parallel, DMA
- Concurrent I/O data transfer
- Modular design for economical expansion

## OPTIONS

- Real-time clock
- Automatic power-fail/restart
- Memory parity
- Memory protect
- Communications interfaces
- Peripheral controllers

OPERATION CODE	MNEMONIC	INSTRUCTION NAME	TIME (microseconds)
0 0	HLT	Halt	5.72
0 1	TRP	Trap	15.84
0 2	ESW	Enter Sense Switches	4.84
0 3	PMP	Protect Memory Page	5.72
0 4	DIN	Disable Interrupt System	4.84
0 5	EIN	Enable Interrupt System	4.84
0 6	DRT	Disable Real Time Clock	4.84
0 7	ERT	Enable Real Time Clock	4.40
0 8	RO1	Reset Overflow and Set Word Length to 1	5.28
0 9	RO2	Reset Overflow and Set Word Length to 2	5.28
0 A	RO3	Reset Overflow and Set Word Length to 3	5.28
0 B	RO4	Reset Overflow and Set Word Length to 4	5.28
0 C	SO1	Set Overflow and Set Word Length to 1	5.28
0 D	SO2	Set Overflow and Set Word Length to 2	5.28
0 E	SO3	Set Overflow and Set Word Length to 3	5.28
0 F	SO4	Set Overflow and Set Word Length to 4	5.28
34	NOP	No Operation	

### Conditional Jump

1 0	JOV	Jump if Overflow Set	Jump	8.58
1 1	JAZ	Jump if A Equal to Zero	Jump	6.82
1 2	JBZ	Jump if B Equal to Zero	Jump	7.70
1 3	JXZ	Jump if X Equal to Zero	Jump	8.14
1 4	JAN	Jump if A Negative	Jump	8.36
1 5	JXN	Jump if X Negative	Jump	8.14
1 6	JAB	Jump if A Equals B	Jump	9.24
1 7	JAX	Jump if A Equals X	Jump	9.02
1 8	NOV	Jump if Overflow not Set	Jump	7.70
1 9	NAZ	Jump if A not Equal to Zero	Jump	8.58
1 A	NBZ	Jump if B not Equal to Zero	Jump	8.36
1 B	NXZ	Jump if X not Equal to Zero	Jump	7.48
1 C	NAN	Jump if A not Negative	Jump	7.26
1 D	NXN	Jump if X not Negative	Jump	7.48
1 E	NAB	Jump if A not Equal to B	Jump	9.24
1 F	NAX	Jump if A not Equal to X	Jump	9.02
			No Jump	8.14

### Shift

2 0	LLA	Logical Left A	5.94
2 1	LLB	Logical Left B	5.94
2 2	LLL	Logical Left Long	5.94
2 4	LRA	Logical Right A	5.94
2 5	LRB	Logical Right B	5.94
2 6	LRL	Logical Right Long	5.94
2 8	ALA	Arithmetic Left A	5.94
2 9	ALB	Arithmetic Left B	5.94
2 A	ALL	Arithmetic Left Long	5.94
2 C	ARA	Arithmetic Right A	5.94
2 D	ARB	Arithmetic Right B	5.94
2 E	ARL	Arithmetic Right Long	5.94

### Input/Output

3 0	IBS	Input Byte Serially	86 ms
3 1	IBA	Input Byte to A	8.36
3 2	IBB	Input Byte to B	8.80
3 3	IBM	Input Byte to Memory	14.30
3 4	NOP		3.52
3 8	OBS	Output Byte Serially	100 ms
3 9	OBA	Output Byte from A	8.36
3 A	OBP	Output Byte from B	9.24
3 B	OBM	Output Byte from Memory	14.52

### Register Operate

4 0	ORA	OR B with A	6.38
4 1	XRA	Exclusive — OR B with A	6.38
4 2	ORB	OR A with B	6.60
4 3	XRB	Exclusive — OR A with B	6.60
4 4	INX	Increment X	7.04
4 5	DCX	Decrement X	7.04
4 6	AWX	Add Word Length to X	7.04
4 7	SWX	Subtract Word Length from X	7.04
4 8	INA	Increment A	7.04
4 9	INB	Increment B	7.04
4 A	OCA	One's Complement A	6.60
4 B	OCB	One's Complement B	6.60
4 C	TAX	Transfer A to X	7.04
4 D	TBX	Transfer B to X	7.04
4 E	TXA	Transfer X to A	7.26
4 F	TXB	Transfer X to B	7.26

## IONS SET

OPERATION CODE	MNEMONIC	INSTRUCTION NAME	TIME (microseconds)
<b>Memory Referencing Instruction</b>			
<b>Fixed Word Length</b>			
6 0	JMP	Jump	3.52
6 8	RTJ	Return Jump	6.38
7 0	IWM	Increment Word in Memory	5.94
7 8	DWM	Decrement Word in Memory	5.94
8 0	LDX	Load X	5.94
8 8	STX	Store X	5.94
9 0	MUL	(Minimum) (Average)	55.66 63.36
		(Maximum)	70.40
9 8	DIV	(Minimum) (Maximum)	83.60 90.86
<b>Variable Word Length</b>			
A 0	ADA	Add to A	5.06
A 8	ADV	(1 Byte) (2 Bytes) (3 Bytes) (4 Bytes)	6.82 6.38 9.46 9.02
B 0	SBA	Subtract from A	5.50
B 8	SBV	(1 Byte) (2 Bytes) (3 Bytes) (4 Bytes)	7.26 6.82 9.90 9.46
C 0	CPA	Compare A	4.84
C 8	CPV	(1 Byte) (2 Bytes) (3 Bytes) (4 Bytes)	4.84 5.72 7.48 8.58
D 0	ANA	And A	5.50
D 8	ANV	(1 Byte) (2 Bytes) (3 Bytes) (4 Bytes)	7.26 6.82 9.90 9.46
E 0	LDA	Load A	5.50
E 8	LDV	(1 Byte) (2 Bytes) (3 Bytes) (4 Bytes)	7.26 6.82 9.90 9.46
F 0	STA	Store A	4.62
F 8	STV	(1 Byte) (2 Bytes) (3 Bytes) (4 Bytes)	3.74 5.06 8.80 10.12

## Addressing Modes

A 0	ADA	Direct Page 0	Add to A—Page 0	5.50
A 1	ADA	Direct Relative	Add to A—Relative	6.60
A 2	ADA*	Indirect Page 0	Add to A—Indirect Page 0	8.80
A 3	ADA*	Indirect Relative	Add to A—Indirect Relative	9.90
A 4	ADA—	Indexed	Add to A—Indexed	5.06
A 5	ADA+	Indexed with Bias	Add to A—Indexed With Bias	5.94
A 6	ADA/	Extended	Add to A—Extended Address	6.60
A 7	ADA=	Literal	Add to A—Literal	
		Fixed Length		7.92
		Two Byte with A		8.36
		Variable		7.92
		Indirect Jumps		10.78

## DATA FORMATS

8 Bits (1 Byte) — Range:  $+2^7 - 1$  to  $-2^7$

Sign Extended	$\pm$	Magnitude	(unused)												
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	3 2 1 0												
A Register								B Register							

16 Bits (2 Bytes) — Range:  $+2^{15}-1$  to  $-2^{15}$

Diagram of the 16-bit floating-point format:

- Sign bit:  $\pm$
- Magnitude: 8 bits (labeled "Magnitude")
- Exponent: 8 bits (labeled "(unused)")

Bit positions (from left to right):

- 15: Sign bit ( $\pm$ )
- 14: 1
- 13: 1
- 12: 1
- 11: 1
- 10: 1
- 9: 0
- 8: 6
- 7: 8
- 6: 5
- 5: 4
- 4: 3
- 3: 0
- 2: 1
- 1: 0
- 0: 15
- 15: 1
- 14: 1
- 13: 1
- 12: 1
- 11: 1
- 10: 0
- 9: 8
- 8: 6
- 7: 5
- 6: 4
- 5: 3
- 4: 2
- 3: 1
- 2: 0
- 1: 1
- 0: 0

Labels: A Register, B Register

24 Bits (3 Bytes) — Range:  $+2^{23}-1$  to  $-2^{23}$

Sign Extended										Magnitude																					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A Register										B Register																					

32 Bits (4 Bytes) — Range:  $+2^{31}-1$  to  $-2^{31}$

## SPECIFICATIONS

- Clock Rate 4.55 mHz (crystal controlled)
- Core Memory 1.1 microsec full-cycle. Modules of 4,096 bytes (8, or 9-bit) to maximum of 32,768 bytes.
- Arithmetic Multiprecision, parallel, binary, fixed point, two's complement.
- Addressing Eight modes including relative, index, indirect, and literal.
- Input/Output 8-bit parallel byte I/O bus for programmed and fully automatic concurrent transfers. Serial I/O interface for teletypes or similar devices. Direct Memory Access (DMA) channel with maximum transfer rate of 909,000 bytes per second.
- Interrupts A priority interrupt system allows internal interrupt on power failure, real-time clock, memory parity error, and external interrupts on the byte I/O bus. Up to 64 interrupts expandable in groups of 8.
- Logic TTL logic elements including MSI types, in DIP ceramic packages. DTL circuitry for I/O interfaces.
- Registers Six operational registers including A-accumulator, B-auxiliary accumulator, X-indexed, P-program counter, W-2-bit word length mode and O-1-bit overflow flag.
- Instructions 89 standard instructions including 17 control, 16 conditional jump, 12 shifts, 8 input/output, 16 register operate, 18 memory reference, 1 multiply, and 1 divide.
- Cabinet The processor, memory to 16K, I/O interfaces, power supply and fan are enclosed in a cabinet 8 $\frac{3}{4}$ " high, 19" wide, and 23" deep. Fully expanded cabinet weighs 75 pounds.
- Power 115/230 vac, 50-60 Hz. 340 watts.
- Environment 0 - 50 C (32 - 122 F)
- Panels The *system control panel* displays all registers, manual command execution, and control switches. The *basic control panel* provides only the basic control switches.
- Software Cross assembler in Fortran IV, Two-Pass Assembler, Teletype Operating System, Tape Editor, CIP/2000 Simulator.

## AVAILABLE PERIPHERAL INTERFACES

- Teletype
- 300 LPS Paper Tape Reader
- DRPE Paper Tape Punch
- 400 CPM Card Reader
- 300 LPM Line Printer
- Tape Cassette
- CRT

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